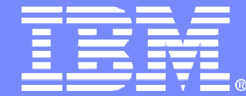

IBM Systems and Technology Group

The Foundry-Packaging Partnership

Enabling Future Performance

Jon A. Casey

IBM Fellow
IBM Systems and Technology Group

5/30/2013

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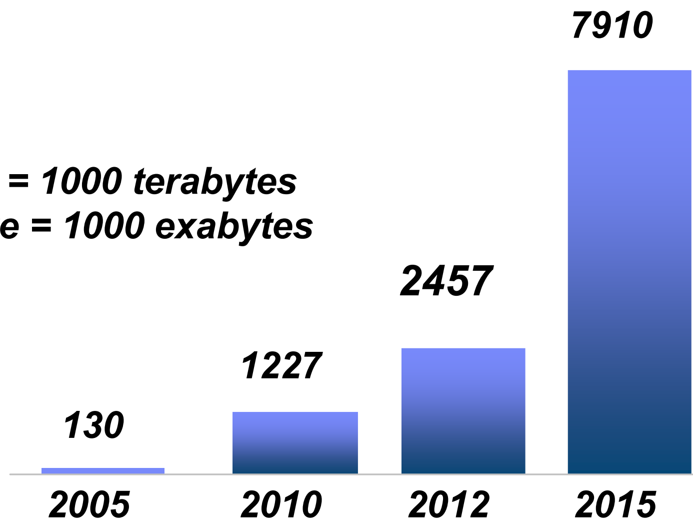
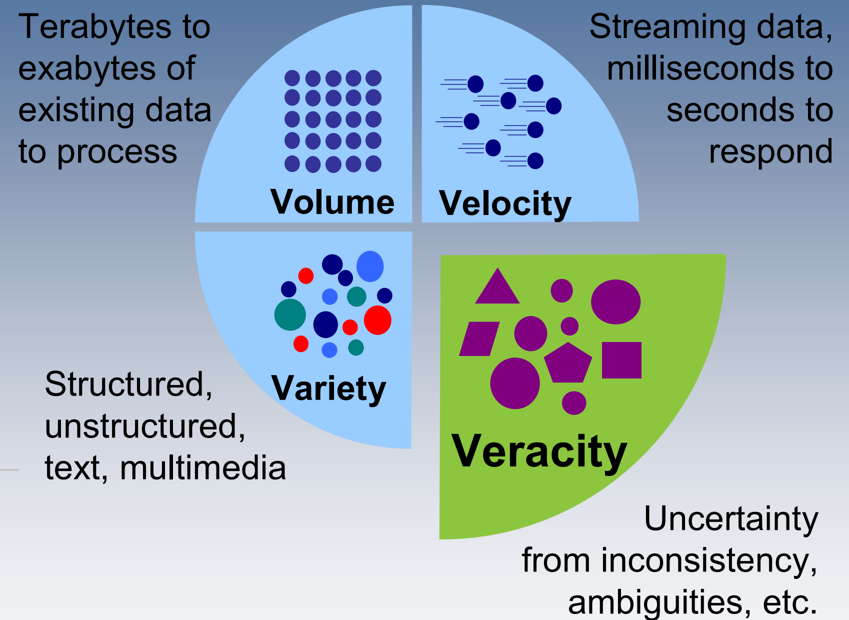
Data growth will drive the new IT model





The Data is in the Cloud !

The Compute will move to the Da

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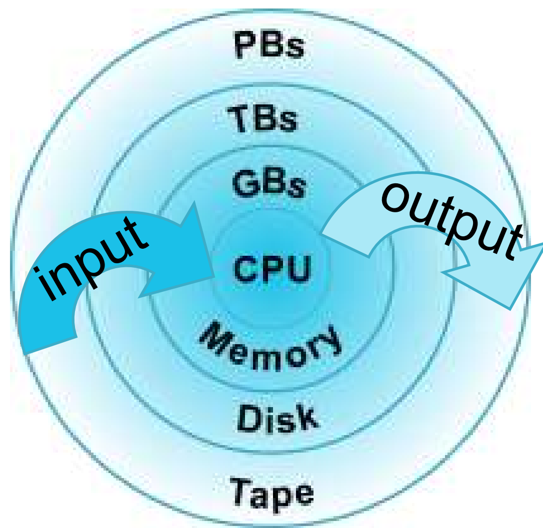
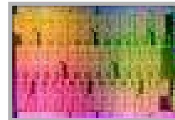
Changes in the compute model –memory centric computing

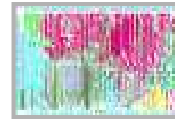
Old Compute-centric Model



Manycore

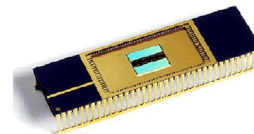


FPGA



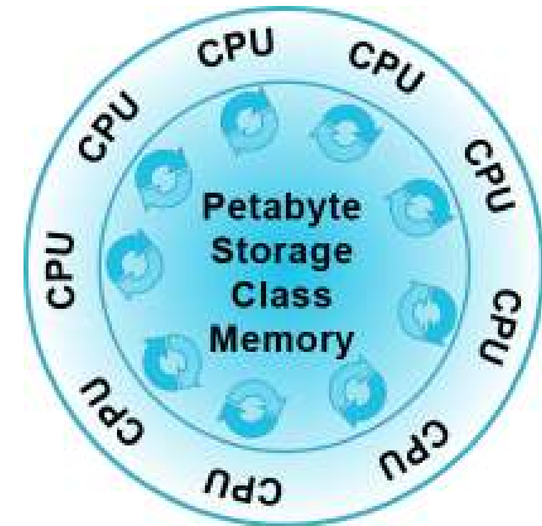
Massive Parallelism
Persistent Memory

Flash



Phase Change

New Data-centric Model



Data lives on disk and tape
Move data to CPU as needed
Deep Storage Hierarchy

Data lives in persistent memory
Many CPU's surround and use
Shallow/Flat Storage Hierarchy

Huge impact on hardware, systems software, and application design

Open Architecture, Software Defined Environment

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Will semiconductor technology alone get us to the goal line?

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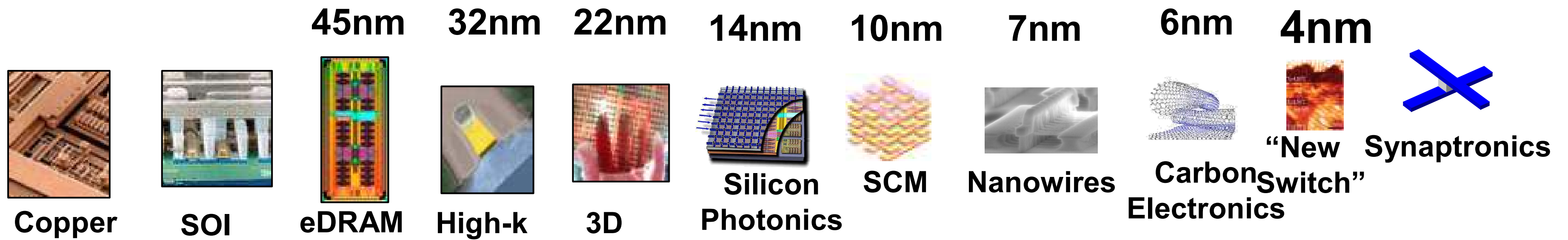
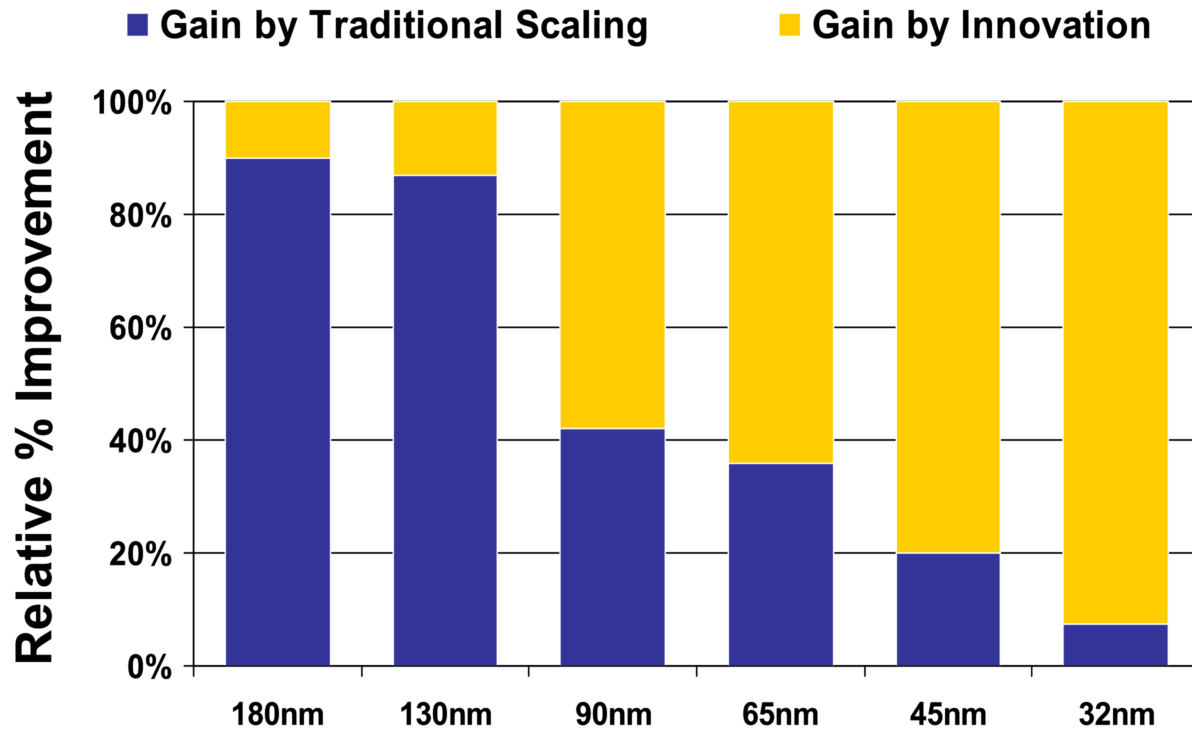


IBM Transistor Performance Improvement



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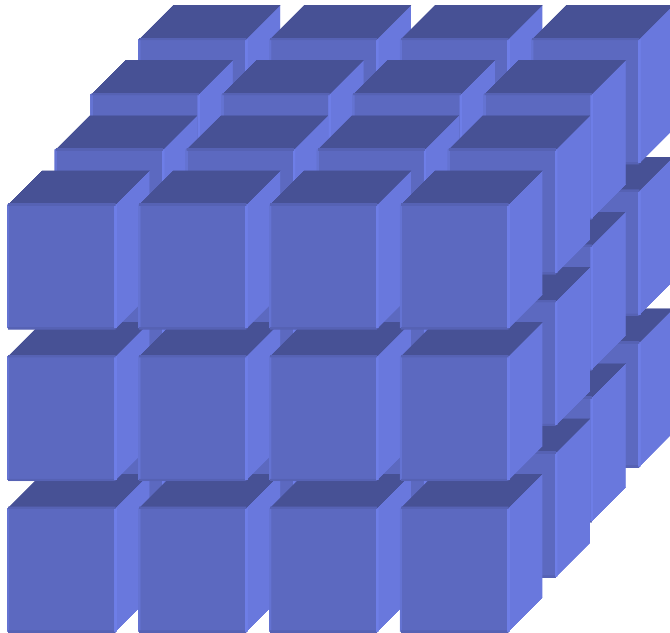
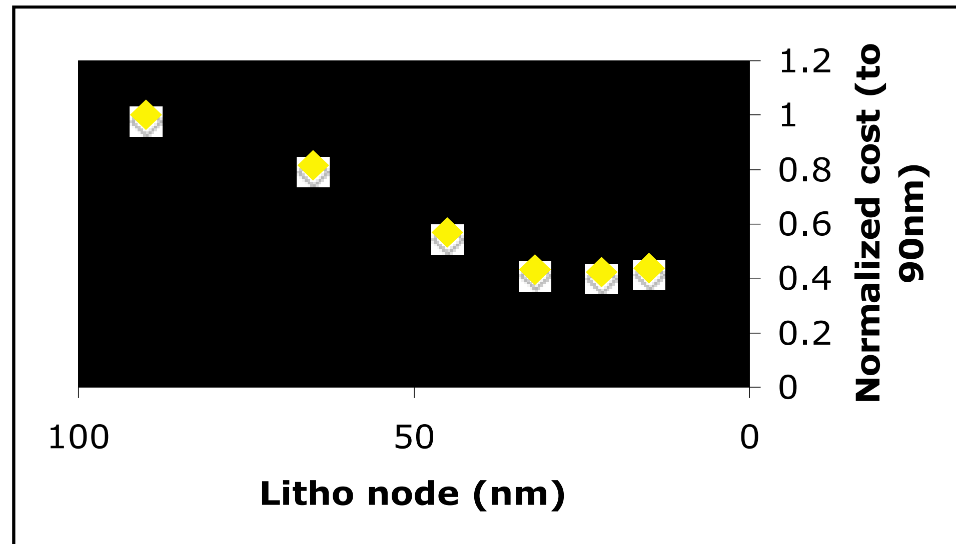


Scaling can and will continue to at least the "7 nm" node

Cost per transistor has begun to saturate



But It will be expensive

No cost-effective lithography

45 nm	32 nm	22 nm	14 nm	10 nm
Immersion (ArFi)	2nd Generation Immersion	3rd Gen ArFi w/ Source Mask Optimization (SMO)	4th Gen ArFi w/ SMO & Double Patterning (DPL)	5th Gen ArFi w/ Multilayer Patterning or EUV

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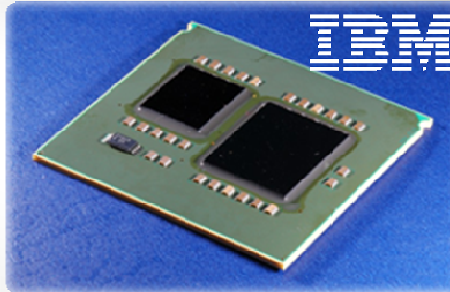
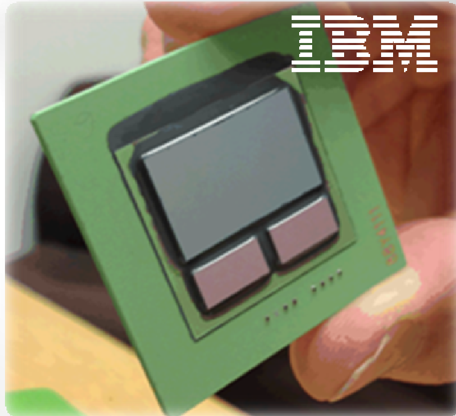
Advanced packaging market trends

- *Slowing of Moore's Law forces higher integration, which leads to larger die*
- *Systems, Networking & mobile architects are moving to higher levels of integration: 3D stacking, 2.5D interposers & MCM*

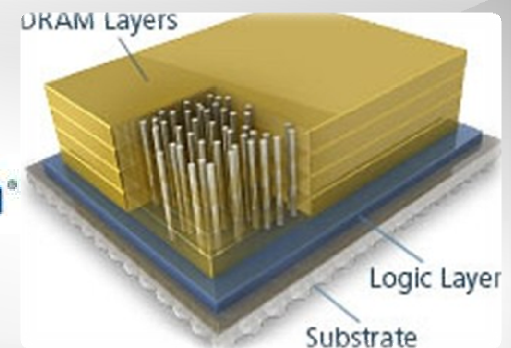
Heterogeneous integration of multiple technologies



Organic DCM



Silicon Interposer



3D TSV

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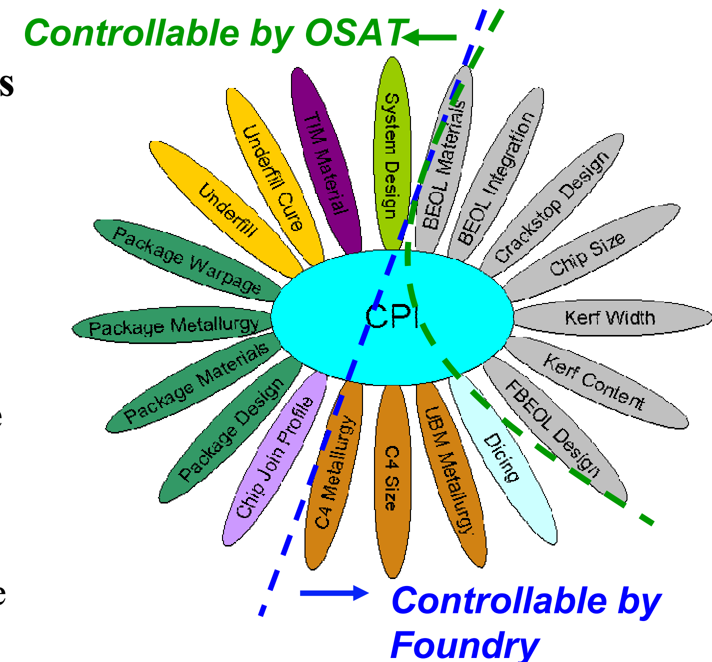
Heterogeneous Integration and 3D*i* : "Volumetric Scaling"

- **Requires co-development of Silicon and Packaging solutions**
  - Packaging is the key technology for volumetric scaling
    - 2D and 3D technologies
    - High performance I/O
    - Optics
    - CPI: Chip-Package Interaction
    - Power and thermal management
- **Provides lower cost solutions to enable system performance**
  - Si cost:performance metric is very challenged
- **Allows for use of mixed semiconductor technologies**
  - Enables use of lower cost technologies for less performance sensitive functions
- **Currently in development at IBM**
  - CSP (chip scale packages)
  - SIP (system in package)
  - Interposers
    - Si and other interposer materials
  - 3D*i*
  - Photonics



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Summary

- **Silicon performance advancement becoming more challenging as scaling is becoming more costly**
  - Need to look beyond CMOS for cost effective technology solutions
- **Integrated co-development of Silicon and Packaging solutions required to achieve new technologies with superior cost:performance metrics**
- **Volumetric scaling will be critical to future performance enablement**
  - Tightly coupled modules and components
  - 3D*i* technology
  - Interposer integration
  - High performance I/O and optics

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